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ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES

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Introduction

Traditionally, integrated circuits packaged in through-hole packages and surface mount packages can be placed directly into Automatic Test Equipment (ATE) for electrical test for reliability tests and production. However, for solder bump based packages, this test method becomes challenging. One alternative method of performing electrical tests and reliability tests is to mount integrated circuits in solder bump based packages onto adapter test boards, which enables the connection between the integrated circuit devices to the biased reliability boards and ATE. Chip-Scale Packages (CSP), Flip-Chip Die that are to be assembled directly to boards, and other Fine-Pitch Packages (FPP) may benefit from use of an electrical test adapter board for component-level reliability testing.

This document provides guidelines on testing of integrated circuit devices mounted on adapter test boards specifically for the purpose of performing reliability tests to identify component-level failure mechanisms. The use of adapter test boards is a lower cost alternative to using custom sockets on the biased reliability boards and ATE interface boards.

This publication recommends that JESD47 or another JEDEC qualification standard be used. This document augments those requirements with guidance on some testing that may be preferable to execute in a format where the supplied device is mounted on an adapter test board either for the purpose of handling efficiency through the reliability stress or electrical test evaluations. The reliability stress test is performed to assess the robustness of the chip-scale, flip-chip, and fine-pitch package manufacturing process and/or to determine whether there are chip-package interaction effects. These considerations apply to devices in chip-scale packaging, flip-chip direct attach, and fine-pitch packages. This document also offers guidelines for mitigating the risk of adapter test-board-related failure mechanisms.

ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES

(From JEDEC Board Ballot JCB-25-25, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication describes guidelines for applying JEDEC reliability tests and recommended testing procedures to integrated circuits that require adapter test boards for electrical and reliability testing. These tests are used frequently in qualifying integrated circuits as a new product, a product family, or as products in a process which is being changed.

Integrated circuit devices in various packages that cannot be tested directly with the Automated Test Equipment (ATE) are each mounted on an adapter test board for testing. Some common devices mounted on adapter test boards for test purposes are Chip-Scale Package, Flip-Chip Die, and Fine-Pitch Package devices (e.g., 64 lead QFN package with 0.50 mil lead pitch).

This document provides guidelines for adapter test board-level reliability tests, recommended testing procedures, test board designs, and construction materials. It is aimed to provide a reproducible assessment of the reliability performance of integrated circuit devices while duplicating the failure modes normally observed during product life cycle. The reliability test recommendations do not apply to the following:

- a) Integrated circuits that are stressed and/or tested in an electrical socket.
- b) WL CSP devices that are stressed and/or tested using a wafer-level probe card.
- c) Second-level solder joint reliability tests such as drop test, thermal cycle test, bend test, etc.

These reliability tests are capable of evaluating and simulating package and device failures in an accelerated manner compared to use conditions. The guidelines prescribed in this publication are not aimed for reliability tests for devices in extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments. Each reliability test should be examined for:

- a) Any potential new and unique failure mechanisms,
- b) Any situation where these tests and/or conditions may induce false failures.

2 Terms and Definitions

adapter test board: A printed circuit board constructed specifically for the purpose of mounting integrated circuits for stress and reliability testing purposes.

NOTE An adapter test board enables the electrical connection between the test equipment and the integrated circuit.

chip-scale package (CSP): A package whose area is generally no greater than 120% of the area of the semiconductor device it contains.

component: A constituent part.

failure: The loss of the ability of a device or component to meet the electrical or physical performance specifications that it was intended to meet.

flip-chip die: An unpackaged die whose interconnection to a substrate is formed through solder joints.

integrated circuit (IC): A circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce.

packaged device: A semiconductor device within an enclosure that allows electrical connections to, and provides mechanical and environmental protection for, that device.

redistribution metallization layer (RDL): Often called “runners” or “traces” that allow re-routing the signal path from the die peripheral input/output (I/O) to an area array of new bump locations, often with significant loosening of effective bump pitches.

sample: A set of individuals taken from a population.

second-level assembly: The attachment of a component to the next level of assembly packaging.

3 **Reference Documents**

IPC-5702, *Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards*

IPC-9701, *Performance Test Methods and Qualification Requirements for Surface mount Solder Attachments*

IPC-TM-650, *Test Methods Manual Method 2.6.3.3 Surface Insulation Resistance, Fluxes*

IPC-TM-650, *Test Methods Manual Method 2.6.3.7 Surface Insulation Resistance*

JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Devices*

JEP154, *Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress*

JESD22-A102, *Accelerated Moisture Resistance – Unbiased Autoclave*

JESD22-A103, *High Temperature Storage Life*

JESD22-A104, *Temperature Cycling*

JESD22-A105, *Power and Temperature Cycling*

JESD22-A110, *Highly Accelerated Temperature and Humidity Stress Test (HAST)*

JESD22-A113, *Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing*

JESD22-B111, *Board Level Drop Test Method of Components for Handheld Electronic Products*

JESD22-B117, *Solder Ball Shear*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

J-STD-012, *Implementation of Flip Chip and Chip Scale Technology*

J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

Telcordia GR-78-CORE, *Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment, Section 13.1.1 and 13.1.2*

4 General Requirements

4.1 Objective

An adapter test board is defined as a Printed Circuit Board (PCB) assembly constructed specifically for the purpose of component-level reliability testing. For adapter test board design considerations and material guidelines, see Clause 5 of this document. Examples of several variations of adapter test board designs are provided in Annex A of this document. Other variations of adapter test boards not provided in Annex A can also be used for the reliability tests described in this document provided that the PCB configurations do not in any way hinder the testing or stressing of the integrated circuit device.

4.2 Stress/Test Parameters

Procedures should be consistent with the requirements of JESD47. This includes, but is not limited to: lot and production recommendations, re-usability of test samples, and definition of electrical test failure after reliability stress.

4.3 Electrical Test

Electrical test equipment with capabilities to perform appropriate testing on devices should be used to test electrical parameters (e.g., data sheet values, in-house specifications, etc.). This may require the use of special electrical test boards and sockets. The electrical tests performed for integrated circuit devices mounted on an adapter test board should be consistent with ones performed for those IC devices at the component level.

5 Adapter Test Board Design

The following design and construction guidelines are recommended for adapter test board reliability tests:

- a) **Clearances** – Adapter test board should allow sufficient space between the IC component and the edge of the adapter test board to simulate the field condition during its product life cycle and to allow for easy handling. A minimum gap of 5 mm is recommended between the IC component and edge of the adapter test board. Adapter test boards with through-hole connectors should be designed to minimize the possibility of contamination of the IC components during the soldering process. A minimum gap size of 3.8 mm between the IC component and the nearest through-hole is required. For both edge connector and through-hole connectors, larger spacing is preferred since it can help alleviate the chance of inadvertent flux contamination.
- b) **Layout** – Adapter test boards should be panelized, when possible, to improve the manufacturability. Panel size should be minimized in order to help ensure highly accurate solder mask registration. Smaller panel size also decreases the risk of warpage during manufacturing.
- c) **Thickness** – Due to second-level solder joint stresses on the device while mounted to an adapter test board during reliability testing, overall board thickness should be carefully considered. Lowering the board thickness will result in a lower overall solder joint stress level. Thinner boards can also result in more warpage, however, resulting in manufacturing difficulties. It is recommended that the thinnest board possible be used that allows for good manufacturing. Customer board thickness should also be taken into account, and adapter test board thickness should match the end application as closely as possible if known. A typical adapter test board nominal thickness is 0.75-1.5 mm. Please note that the board thickness may be fixed based on the mating connectors/sockets in all cases with the exception of through-hole type of adapter boards.
- d) **Layers** – There is no requirement for number of layers in the adapter test board design, although some typical guidelines can be followed. The lowest cost option will be a 1-2 layer design, and is most likely suitable in most situations (especially lower pin count packages). The copper distribution should be as symmetrical as possible in all axes to minimize warpage. Two layer boards are preferred since one layer boards w/asymmetric metal traces are more prone to warpage. The preference is to have a two layer board with metal traces, which are balanced at the top and bottom of the board.
- e) **Vias** – The usage of vias should be minimized when possible. If vias are employed to establish connections, larger vias are preferred for better manufacturability during the plating process. If via-in-pad connections are necessary, it is recommended that the vias be filled and planarized. For space reasons, microvias may need to be considered, which should be filled for smaller pitch package connections.
- f) **Connectors** – Edge connectors, surface mount headers, or wave solder connector, are recommended for adapter test boards to facilitate connection to a test system.

5 Adapter Test Board Design (cont'd)

- g) **Materials** – Adapter test boards should be constructed with reliability test grade materials. Other adapter test board materials can be used providing they have previously passed reliability stress without fail. All soldering materials such as solder pastes and fluxes used in the test should be Surface Insulation Resisted (SIR) tested in advance to ensure chemical compatibility. Adapter test boards should be constructed with an appropriate PCB board material suitable for Pb-free processing. With advent of low-halogen laminates in deference to FR4 laminates, it may be important to characterize whether selected laminate can affect the response of the adapter test board. The adapter test board material should have a datasheet rating such that it can meet the temperature and humidity requirements associated with the chosen temperature cycling and HAST test conditions.
- h) **Components** - On a single adapter test board, one or more IC components can be mounted. For a single IC component on an adapter test board, the IC component should be centered on the adapter test board. When multiple IC components are mounted on the same adapter test board, they should be arranged in a symmetrical array pattern centered on an adapter test board. The recommended minimum spacing between the edge of the card and an IC component should be at least 5 mm.
- i) **Surface Finish** - Organic Surface Protection (OSP) is the preferred surface finish for the IC component mounting pads on the adapter test boards. Other lead-free compatible planar surface finishes may be used if needed. Alternates include Immersion Silver (ImmAg), Immersion Tin (ImmSn), Electroless Nickel Immersion Gold (ENIG) and Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG). It should be noted that the reliability results on finishes that form Copper-Tin Intermetallics (OSP, ImmAg and ImmSn) may differ from those on finishes that form Nickel-Tin Intermetallics (ENIG, ENEPIG), so the choice of adapter test board finish should take into account the most likely finish in the end-use application where this is known. Exception: for the biased/moisture environmental tests (i.e. THB and Biased HAST) NiAu plating and no solder stop mask is recommended to mitigate the risk of copper migration during the stress.
- j) **Edge Connector material** - For adapter test boards with edge tabs, selective plating of a different finish on the edge tabs may be necessary to prevent corrosion or oxidation of the edge tabs and to ensure good contact between the edge tabs and the connectors in the test system. A common edge tab finish is electrolytic Nickel Gold. For edge fingers with staggered rows of fingers a common finish is ENIG or similar material.
- k) **Underfill** – May be utilized to strengthen the attachment of the integrated circuit to the adapter test board, and lessen the occurrence of test artifacts and other unwanted responses unrelated to failures modes in the IC devices. Use of underfill may require understanding of the adhesive properties to ensure that it is compatible with the reliability stresses. If an underfill process is included a cleaning process is also recommended to remove flux residues.

6 Recommended Reliability Tests

6.1 General Tests

JESD47 defines the primary IC component qualification reliability requirements. When an adapter test board is used to evaluate the reliability of an IC component the preconditioning can be performed either before the board mounting process or after. Both options are outlined in the subsequent clause. Electrical testing should be performed per JESD47.

6.2 Mounting IC Components on Adapter Test Boards and Preconditioning Recommendations

The preconditioning test procedures should be consistent with the requirements per JESD22-A113, especially Clause 5.6.1 of that standard (5.6.1 - Solder Attachment After Reflow).

The JESD47 recommended sample size of units mounted on adapter test boards are needed. These samples will be used to accommodate the subsequent TC, HTSL, HAST or THB or UHAST tests.

Components can go through the preconditioning process either before or after being mounted onto the adapter test boards with the appropriate reflow condition as specified in the device procurement document if applicable.

If preconditioning is done before mounting, it is recommended to perform the initial electrical functional/parametric testing prior to the board mount process. After board mount the electrical functional/parametric testing should be performed on the adapter test-board-level integrated circuit devices prior to the reliability stress conditions. All failures found after the post-board mount electrical test can be classified as assembly defects and replaced as long as failure analysis work is performed to validate the failures are an artifact of the board mounting process and not a device issue.

If preconditioning is done after mounting, the adapter test boards must be capable of withstanding the moisture soak and reflow process. The adapter test boards can either be singulated prior to or after the completion of the mounting process. It is recommended to mount integrated circuit components onto panelized adapter test boards and use a de-panelize process which is not generating stress on the board.

Perform initial electrical functional/parametric tests to verify that the units mounted on singulated adapter test board panels meet the room temperature data sheet specification. Replace units that fail to meet this requirement after initial electrical test to maintain the recommended sample size.

After the completion of initial electrical test, perform a visual inspection of the integrated circuit devices mounted on adapter test board after the assembly process to locate defects. Replace defective units with passing units to maintain the recommended sample size. Defective units should undergo failure analysis to validate the failures are an artifact of the board mounting process and not a device issue.

6.2 Mounting IC Components on Adapter Test Boards and Preconditioning Recommendations (cont'd)

Upon the completion of visual inspection, moisture soak should be performed according to the expected MSL levels as prescribed in JESD22-A113 as determined using J-STD-020. In some cases such as dealing with small CSP devices where little or a small amount of moisture absorption is expected, time duration for the moisture soak can be reduced if the moisture absorption is verified to have reached saturation, e.g., based on weight gain analysis (absorption) as described in J-STD-020.

After the completion of moisture soak, two (2) additional reflow cycles are required. Perform reflow of the appropriate conditions and procedures as prescribed in JESD22-A113. Please note that IC components mounted on adapter test boards have already finished one cycle of solder reflow during the mounting process prior to initial electrical test.

A final inspection with X-ray and/or optical microscope is recommended on all CSP devices to check for delamination after the RDL process is completed. Using CSAM has proven to be ineffective in revealing delamination in the finished units due to the layout and size of the solder bump. For details regarding external visual inspection criteria, see Annex B for reference.

Post reliability stress electrical test should be performed per JESD47. Failure analysis is highly recommended to determine the root cause failure mechanism.

6.3 Temperature Cycling (TC) Recommendations

The temperature cycling test procedure should be consistent with the requirements per JESD22-A104.

Devices that fail post temperature cycling electrical test are counted against the reliability test. Failure is defined as per JESD47. For fails, failure analysis is highly recommended to determine the root cause failure mechanism.

For integrated circuit components mounted on adapter test boards for TC testing, rapid thermal expansion and contraction may create excessive stress on the microvias within the PCB and cause false failure. The primary intent of this reliability test is to evaluate the thermal stress performance of the integrated circuit component and not the adapter test board false rejects, which may create additional obstacles for failure analysis.

6.4 Highly Accelerated Stress Test Recommendations

HAST is the preferred reliability test to assess the temperature and humidity effect on the reliability performance of integrated circuit devices mounted on adapter test boards. The HAST test procedure should be consistent with the requirements per JESD22-A110. The sample size, non-consecutive lot, and preconditioning requirements are per JESD47.

HAST is performed to evaluate the reliability of integrated circuit devices in humid environments. For devices mounted on adapter test boards, it is recommended to perform HAST with the following conditions: 110 °C dry bulb temperature, 85% humidity for 264 hours. It is further recommended to perform a cleaning process in order to insure complete flux removal prior to stress.

6.4 Highly Accelerated Stress Test Recommendations (cont'd)

The alternate test condition prescribed in JESD22-A110 using 130 °C dry bulb temperature, 85% humidity for 96 hours is also suitable for the stress condition. However, due to the elevated temperature, oxidation on the solder bump surface may occur and induce false rejects. Some failure mechanisms that could be caused by inappropriate stress conditions are open vias, delamination, adapter test board warping, dendritic growth underneath the solder bumps, solder bump surface oxidation, resistance change, etc. To overcome contact issues a land-pad contactor design can be considered.

Failure is defined as per JESD47. Failure analysis is recommended to determine the failure mechanism.

6.5 High Temperature Storage Life Recommendations

The HTSL test procedure condition should be consistent with the requirements per JESD22-A103.

The sample size and non-consecutive requirements are per JESD47. The appropriate storage temperature and duration should be used. It is necessary to assess the bill-of-material of the integrated circuit device and adapter test board to determine an appropriate stress conditions to avoid damaging the test samples, which could cause false fails.

Failure is defined as per JESD47. Failure analysis is recommended to determine the failure mechanism.

6.6 High Temperature Operation Life Recommendations

The high temperature operation life test procedures should be consistent with the requirements per JESD47.

6.7 Nonvolatile Memory Endurance Cycling and Data Retention Recommendations

The NVM endurance cycling procedures should be consistent with the requirements per JESD47.

6.8 Failure Analysis Recommendations

For integrated circuit devices mounted on adapter test boards that failed reliability tests, failure analysis is highly recommended to determine the root cause mechanism. Failures could be within the component under qualification or within the adapter board itself. Use non-destructive failure analysis techniques on the failures prior to removing the IC components from the adapter test boards. Non-destructive failure analysis techniques may include but not limited to X-Ray analysis, optical inspection, CSAM, Time Domain Reflectometry (TDR), and resistance measurement.

After the units are removed from the adapter test boards, standard failure analysis techniques can be used to isolate the failure mechanism, which may include but not limited to Light Emission Microscopy (LEM), Transmission Electron Microscopy (TEM), and micro-probing.

Annex A (Informative) Examples of Adapter Test Board Designs

Design #1

Description – Single-sided edge connector style board. Land pads are redistributed to the edge connector pads. Connector pads should be Ni/Au plated to prevent excessive wear from multiple inserts into the connector, as well as to prevent pad oxidation that may prevent good contact. Land pad finish can be Cu OSP or Ni/Au, but for the biased-moisture tests Ni/Au is recommended. Solder mask registration around land pads are critical, and should be well centered.

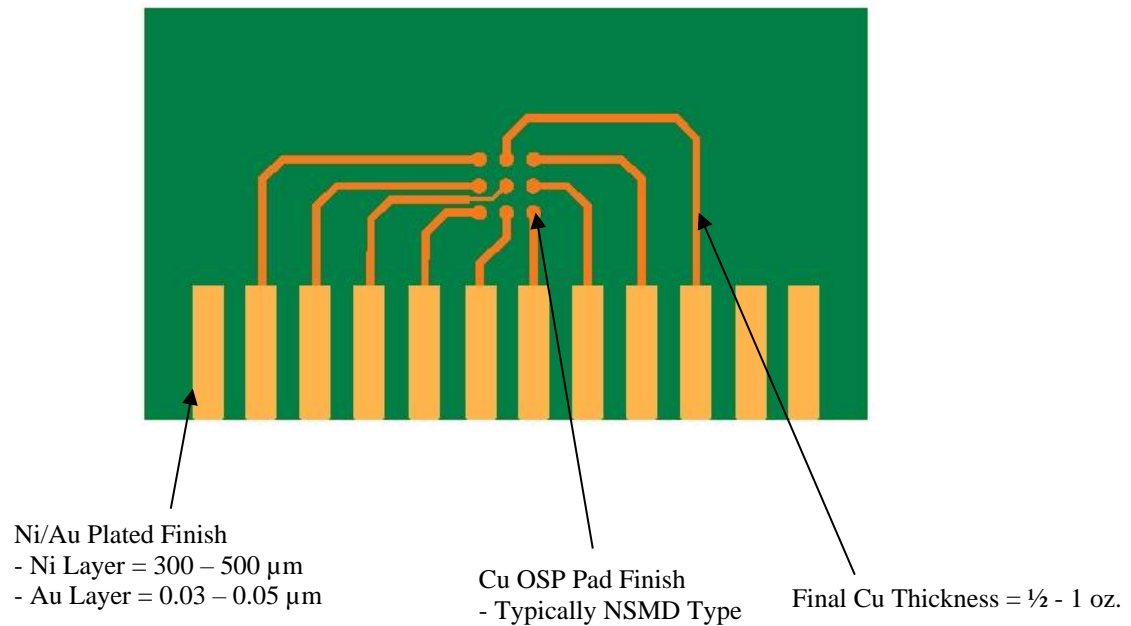


Figure 1 — Configuration of Edge-connector-type Adapter Test Board

Annex A (Informative) Examples of Adapter Test Board Designs (cont'd)

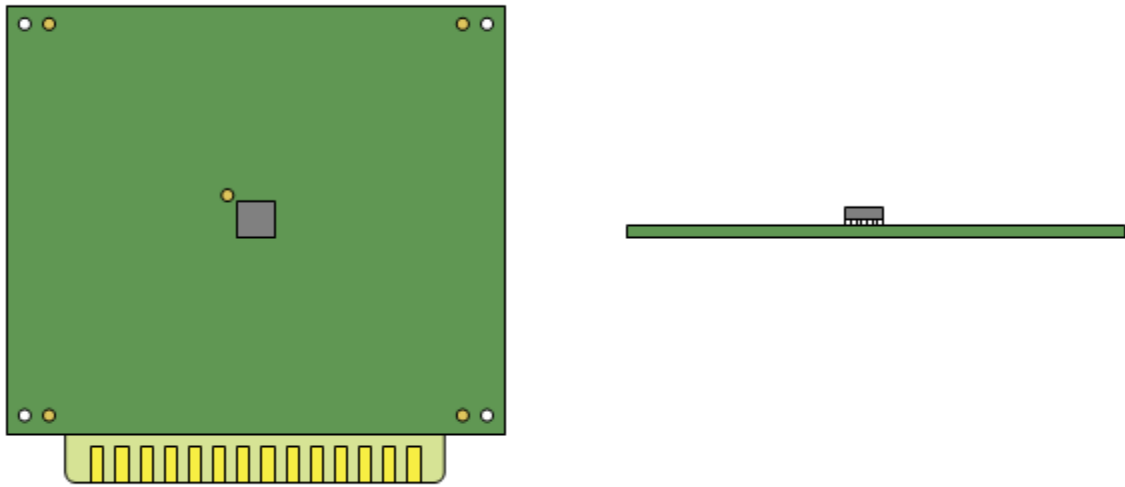


Figure 2 — Configuration of a Single-component Edge-type Adapter Test Board

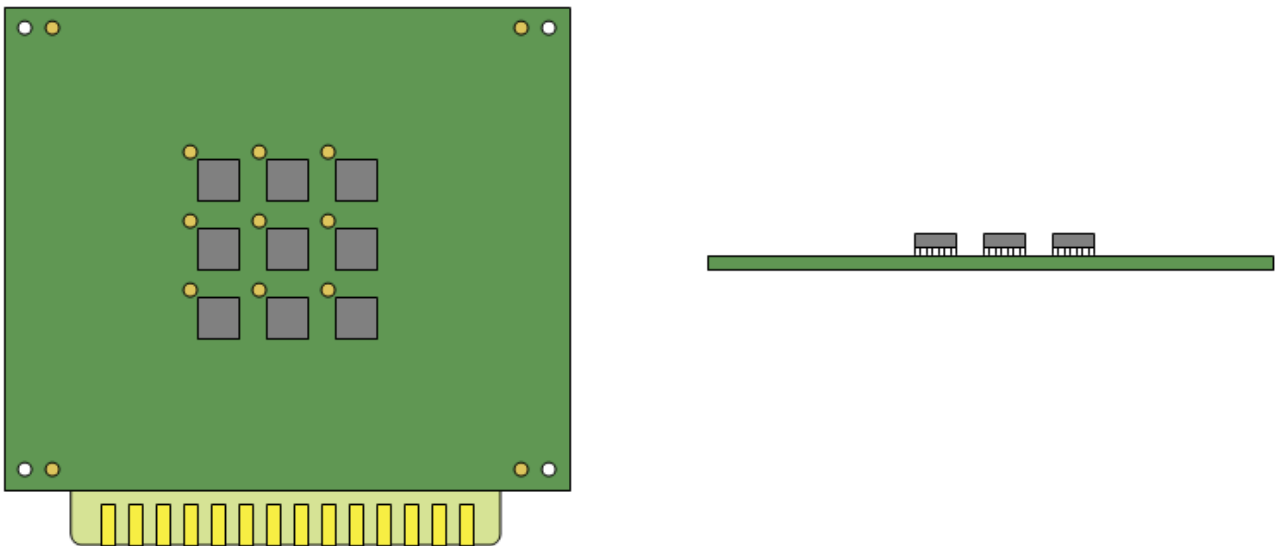


Figure 3 — Configuration of a Multiple-IC Edge-type Adapter Test Board

Annex A (Informative) Examples of Adapter Test Board Designs (cont'd)

Design #2

Description – 4-sided socket style connector. Land pads are redistributed to perimeter connector pads, and the board is typically placed face down in the socket. The socket design should be depressed to prevent inadvertent device contact with the socket bottom. Connector pads should be Ni/Au plated to prevent excessive wear from socket pins through multiple inserts, as well as to prevent pad oxidation that may prevent good contact. Land pad finish is recommended to be Cu OSP for best performance, but Ni/Au is also acceptable. Solder mask registration around land pads are critical, and should be well centered.

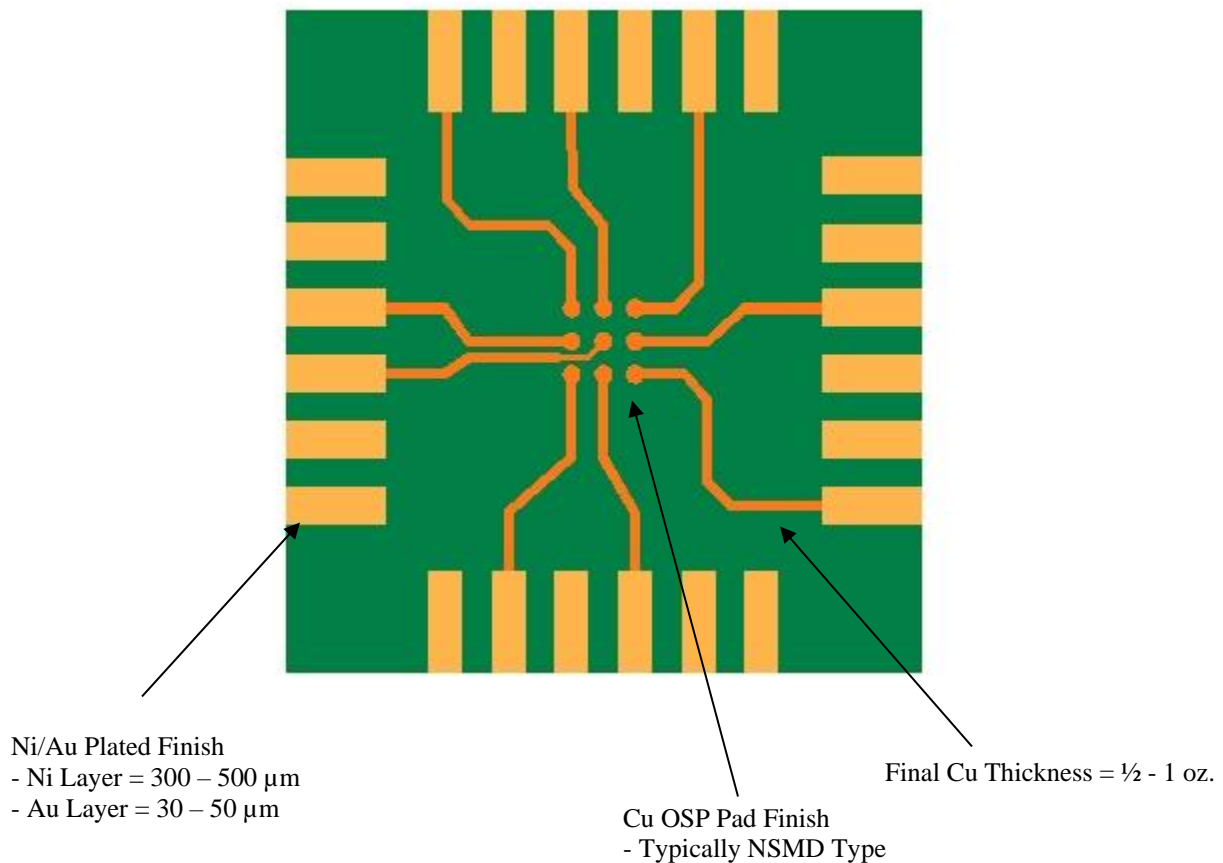


Figure 4 — Configuration of a 4-sided Socket-style Connector

Annex A (informative) Examples of adapter test board designs (cont'd)

Design #3:

Description - For through-hole-type adapter test board, the IC component is mounted on one side of the adapter test board with through-hole leads on the other side (resembles PDIP, TQFP land pattern/footprint, etc.). This enables socketing the integrated circuit device into reliability load boards and automated test equipment. Figure 5 provides an illustration of this configuration.

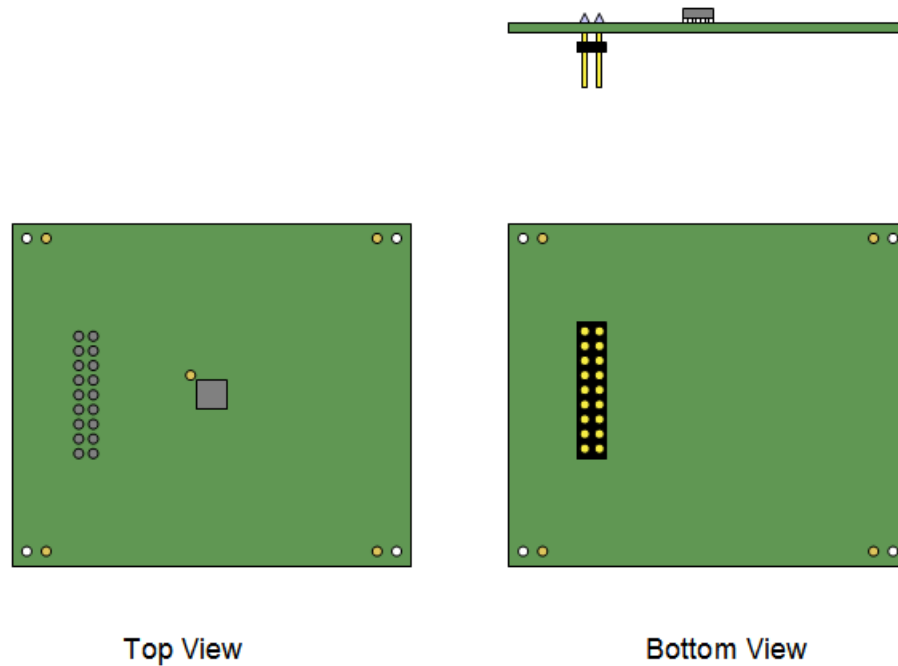


Figure 5 — Configuration of a Through-hole-type Adapter Test Board

Annex B (Informative) Optical Inspection Criteria

The purpose of optical inspection is to verify the workmanship of devices after the preconditioning. A final visual inspection shall be performed after all preconditioning procedures are completed.

Perform an external visual inspection using an optical microscope (at 40X magnification) to look for external defects, which may include but not limited to the following:

1. External cracks:
 - a. External cracks on the die surface
 - b. External cracks on the solder bump or lead surface
 - c. External cracks on the adapter test board
2. Discoloration:
 - a. Discoloration due to corrosion on the die surface (DUT)
 - b. Discoloration due to delamination (DUT)
 - c. Discoloration of the adapter test board laminate, particularly near IC components or circuitry
3. Peeling:
 - a. Peeling of the backside laminate layer for CSP devices
4. Excessive Flux
5. Deformity on the adapter test board
 - a. Warping
 - b. Blistering
6. Severe oxidation of solder balls or leads
7. Dendritic growth between the solder balls, leads or between adjacent traces
8. Corrosion of adapter test board traces, solder joints, or metalized surfaces of the IC components
9. Evidence of pads lifted off the adapter test board laminate
10. Chipping of IC component corners or other physical damage to IC components

Higher magnification of optical microscope can also be used to verify the defects. Boards with external defects should be replaced with passing adapter test boards before continuing with reliability tests.

Annex C (Informative) Differences between Revisions

This annex describes most of the changes made to entries that appear in this standard, JEP176A. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

C.1 Differences between JEP176A and JEP176

This clause briefly describes most of the changes made to entries that appear in this standard, JEP176A, compared to its predecessor, JEP176 (January 2018). Spelling corrections made in this standard are not reported in this summary.

Clause	Description of changes
All	This standard was brought into style/formatting compliance with the latest style standard, <i>Style Manual for Standards and Other Publications of JEDEC</i> , JM7A (July 2024). Front pages and the Feedback Form were updated to their latest versions.
TOC	Added a list of Figures to the Table of Contents.
Introduction	Editorial change to remove dashes in “solder bump based packages”.
1	Editorial change to remove dashes in “64 lead QFN package with 0.50 mil”.
3	Re-ordered the list of reference documents into alphabetical order by document number. Editorial change for JESD22-A113 to capitalize “Mount”. Added reference JEP150.
4	4.1 - Editorial change to capitalize “Annex”, and replaced “section” with “clause”.
5	5 c) and 5 k) - Editorial change from “Maybe” to “May be”. 5 e) – Editorial change from “μVia” to “microvia”.
6	6.1 – Replaced “section” with “clause” 6.2 - Editorial changes to specifically call out Clause 5.6.1 from JESD22-A113, and to capitalize “Annex B”. 6.3 – Editorial change to remove the dash in “microvias”.
Annex A	Design #2 - Editorial change from “Four sided” to “4-sided”, consistent with Figure 4 title.

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STANDARD IMPROVEMENT FORM**JEDEC****JEP176A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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The referenced clause number has proven to be:

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☐ Other _____

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